REMARKS

Claims 1-49 were pending in the application. By this paper, Applicant has amended Claims 1-5, 7-9, 11-20, 22-31, 33-38, 40-42, 44-46, and 48-49, and added new Claim 50. Hence, Claims 1-50 are presented for examination herein.

*Request For Supervisory Interview and Review*

For reasons set forth below, Applicant hereby respectfully and formally requests a personal and/or telephonic interview between the Applicant (including the inventor, Dr. Eric M. Dowling) and the Examiner's Supervisor regarding the instant application, as well as two closely related applications (U.S. Serial No. 10/074,705 filed February 13, 2002, and Serial No. 10/001,007 filed November 14, 2001). Applicant requests that such interview(s) be conducted at the earliest opportunity convenient to the Examiner's Supervisor.

Applicant further formally requests the Examiner's Supervisor to become substantively involved in the details of this examination, and perform a detailed review Office Actions in this application from this point forward. Applicant respectfully submits that many claims as previously presented clearly defined allowable subject matter over the art of record, yet were summarily rejected on what Applicant believes are specious legal and technical bases.

Applicant specifically herein reserves the right to appeal to the board of Administrative Patent Judges.

*Amendments to the Title*

In response to Par. 3 of the Office Action, Applicant respectfully traverses the Examiner's assertion that the previously presented title lacks descriptiveness. The term "Embedded-DRAM-DSP Architecture" is completely descriptive of the broadest generic embodiment of the invention. Requiring Applicant to further include specific attributes or limitations from its claims is an unnecessary restriction on Applicant's right to claim its invention broadly; such additional limitations in the title potentially affecting the claim scope afforded to Applicant.

It is well settled precedent that a patentee is in no way limited to specific embodiments set forth in its specification, and Applicant submits that the inclusion of further aspects of certain embodiments of its invention as requested by the Examiner violates the foregoing well-settled principle.

However, by this paper, Applicant has amended the title of the Application to be as descriptive as possible without unduly limiting or affecting the genericism of the title (and hence potentially the claims).

*Amendments to the Specification*

By this paper, Applicant has amended the Abstract of the Invention in order to more clearly set forth the invention, and to comply with the 150-word limit.

Pursuant to Pars. 5-7 of the Office Action, Applicant has herein amended various portions of the specification in order to correct the reference numeral deficiencies cited by the Examiner. No new matter has been added by these amendments.

*Amendments to the Drawings*

Also pursuant to Pars. 5-7 of the Office Action, Applicant has herein amended Figs. 2 and 4 of the specification in order to correct the remaining reference numeral deficiencies cited by the Examiner not addressed by amendment of the specification. No new matter has been added by these amendments.

Regarding Par. 8 of the Office Action, Applicant traverses the Examiner's assertions and drawing objections set forth in this Paragraph in their entirety. Applicant submits that the Examiner is both (i) misinterpreting 37 CFR 1.83 by strictly requiring <u>every</u> element of <u>every</u> claim to be shown in a Figure, including effectively ignoring the several caveats to the general rule set forth in 37 CFR 1.83 and other relevant statutes/guidance; and (ii) ignoring components which are present in the drawings as filed which perform the precise functions/elements which the Examiner asserts are missing from the claims. Specifically:

(i) 37 C.F.R. § 1.83 states:

*§ 1.83 Content of drawing.*

*(a) The drawing in a nonprovisional application must show every feature of the invention specified in the claims. <u>However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, **should** be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation</u> (e.g., a labeled rectangular box).*

MPEP 608.02 states:

> *"Any structural detail that is of sufficient importance to be described should be shown in the drawing. (Ex parte Good, 1911 C.D. 43, 164 O.G. 739 (Comm'r Pat. 1911).)"* {Emphasis added}

Applicant notes that: (i) the aforementioned passage of MPEP 608.02 does not say "***must*** be shown", and (ii) the passage qualifies the requirement of illustration in the drawing to those details of sufficient importance. **Under the Examiner's overbroad assertions of Par. 8 of the Office Action, every limitation of every claim must be shown in the drawings (irrespective of its importance), and this position is clearly in contravention of 37 CFR §1.83 and MPEP 608.02.**

Furthermore, the Examiner's logic is flawed when considering hypothetical claims that are comprised of only know or "conventional" elements, yet which are combined in a novel and non-obvious way (and clearly patentable under Supreme Court precedent). Again, the Examiner's interpretation of 37 CFR 1.83 in such a case would yield a result in clear contravention of the aforementioned statutes and rules; i.e., by requiring explicit drawing of elements which are clearly "conventional" and hence not required to be drawn with any specificity per the CFR's and statute.

35 USC §113 states:

> *35 U.S.C. 113 Drawings.*
>
> *The applicant shall furnish a drawing where necessary for the understanding of the subject matter to be patented.*

Hence, per the statute, the presence of a drawing of any kind (let alone individual elements thereof) is not required when it is not necessary for the understanding of the subject matter.

Clearly, the Examiner had more than sufficient understanding of all the claimed inventions so as to generate a forty-nine (49) page Office Action, including facially detailed rejections of each claim. Applicant admittedly fails to see how the Examiner can compel the Applicant to submit additional or revised drawings, ostensibly since they are "necessary" under 35 USC §113 and 37 CFR §1.83 for greater understanding, yet clearly have no trouble understanding any portion of the specification or claims during substantive examination.

(ii) Notwithstanding (i) above, Applicant herein traverses the Examiner's assertions that all elements of the claimed inventions cannot be found in the drawings as filed.

For example, Applicant notes the following exemplary passage in the specification regarding "pre-charging" (cited by the Examiner in Par. 8 of the Office Action):

> "*When conditional execution and branching create uncertainties as to what data will be needed, the data and assembly unit may speculatively* ***precharge*** *DRAM rows and/or speculatively prefetch data to be used by the functional units 128.*"
> Page 25, lines 12-15, discussing Fig. 1; emphasis added.

Figs. 1 and 2 clearly show the data/assembly unit 122 which performs the pre-charging operation as described above.

Similarly, regarding "deactivation" (also cited by the Examiner as an example of an element missing from the drawings), page 26 of the specification states in discussing Figs. 1, and 2-4:

> *"As will be discussed in greater detail below in connection with FIGS. 2-4, the* ***data assembly unit 122*** *is operative to control the DRAM arrays using a set of row-address pointer registers. A set of activation bits is manipulated under program control* ***to activate or deactivate entire rows of selected DRAM banks*** *in the DRAM arrays 102, 104, 106."*

Regarding "accessibility" (cited by the Examiner in Par. 8), page 24 of the specification states:

> *"The selector 120 can switch different ones of the register files 112, 114, 116 to be the architectural register file. A selected register file is said to be an active register file. A deselected register file register file is* ***not accessible*** *to the functional units 128 and is said to be an inactive register file."*

Figs. 1 and 2 clearly show all architectural elements necessary to select and deselect register files (including making them "accessible" or "inaccessible").

Regarding the Examiner's citation of the ostensible lack of a drawing showing the "instruction set" (see again Par. 8), Applicant submits that this requirement is (a) nonsensical (i.e., would the Examiner have the Applicant somehow "draw" individual instructions or sets thereof? How does one draw an ephemeral set of electrical impulses, which is what an actual physical implementation of an "instruction" as claimed comprises?); and (b) even if, *arguendo*, the requirement were properly lodged (which Applicant believes it is not), the "instruction set" is

a well known and "conventional" feature (see 37 CFR §1.83) which is already illustrated as shown in the form of a "rectangular box" in, *inter alia*, Fig. 1, Reference numeral 124 (instruction cache), Fig. 5, reference numeral 508, and Fig. 6, reference numeral 608 (showing a plurality of exemplary VLIW instructions or "cache lines").

Applicant submits that it has a "rectangular box" for each and every component of its claimed inventions.

Based on the foregoing, Applicant respectfully submits that each of the Examiner's objections of Par. 8 of the Office Action are completely without merit, and requests that they be withdrawn in their entirety.

*Claims Objections and §112 Rejections*

Pursuant to Pars. 9-39 of the Office Action, Applicant has herein amended various of the claims cited by the Examiner in order to correct the deficiencies cited by the Examiner, as well as various other editorial amendments identified by Applicant during its review of the claims.

Regarding Claims 16 and 20 (see Par. 33 of the Office Action), Applicant has amended Claim 20 to refer to the first and second instruction sets as "sets of instructions" so as to differentiate over the "instruction set" recited in Claim 16.

Applicant notes, however, that the Examiner's original reasoning in this regard is flawed; the terms as previously presented (i.e., first and second instruction sets") are perfectly clear in that they distinguish over the term "instruction set" of Claim 16. As an analogy, it is completely proper to claim "A car having a set of wheels", and subsequently in a dependent claim recite "first and second sets of wheels", and again refer to the first-recited "set of wheels", the latter which may or may not include the former. For example, the first set of wheels may be the two front wheels of the car, and the second set the two back wheels, each having a unique feature (i.e., location on the car) that is not generic to the recited "set of wheels" of the independent claim. The "set of wheels" recited in the independent claim may also include wheels not present in either the first or second sets (e.g., two spare wheels in the trunk). The terms "instruction set", "first instruction set", and "second instruction set" are all unique and differentiable.

Applicant submits that all objections and §112 rejections have been overcome by its amendments presented herein.

*Rejections under 35 U.S.C. §103*

In response to the Examiner Section 103 Rejections of Claims 1-49 as set forth in Pars. 40-92 of the Office Action, Applicant provides the following.

1) Traversal of All "Official Notice"

By this paper, Applicant traverses all explicit and implicit "Official Notice" taken by the Examiner in the Office Action per, *inter alia*, MPEP 2144.03C, and requests the Examiner to present documentary evidence of the prior art on which to base his obviousness rejections, or to withdraw all such improper rejections currently standing in this application.

(i) **Non-judicious use of Official Notice** - MPEP 2144.03 states in relevant part:

> *"In limited circumstances, it is appropriate for an examiner to take official notice of facts not in the record or to rely on "common knowledge" in making a rejection, however such rejections should be judiciously applied.*
> ...
> *The standard of review applied to findings of fact is the "substantial evidence" standard under the Administrative Procedure Act (APA). See In re Gartside, 203 F.3d 1305, 1315, 53 USPQ2d 1769, 1775 (Fed. Cir. 2000). See also MPEP § 1216.01.*
> ...
> *While "official notice" may be relied on, these circumstances should be rare when an application is under final rejection or action under 37 CFR 1.113. Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known. As noted by the court in In re Ahlert, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970), the notice of facts beyond the record which may be taken by the examiner must be "**capable of such instant and unquestionable demonstration as to defy dispute**" (citing In re Knapp Monarch Co., 296 F.2d 230, 132 USPQ 6 (CCPA 1961))."* {Emphasis added}

The Examiner has explicitly utilized "Official Notice" as a basis of rejection in no less than twelve (12) separate instances within the Office Action (**including at least once in each of eight (8) independent claims presented, thereby causing Official Notice to be a substantive basis**

**of all rejections of all claims, dependent and independent, previously presented**), and further has implicitly used Official Notice in numerous other instances (e.g., using the word "inherent" and variations thereof). Applicant submits that this cannot in any way be considered "judicious application" in "limited circumstances" as required by the MPEP.

Applicant notes for example that the Examiner has utilized three (3) references (Inagami, Parady and Bissett) and two Official Notices (Claim 28 and 40) in concocting his basis for rejection of Claim 40; hardly a judicious use in limited circumstances.

Hence, the Examiner's repeated use of Official Notice in all forms (i.e., explicit and implicit) immediately renders his obviousness rejections suspect on, *inter alia*, both procedural and substantive grounds.

(ii) **Improper Use of "Official Notice" as Principal Evidence of Obviousness** – In addition to the foregoing, the Examiner improperly uses such explicit or implicit Official Notice as a critical or principal basis of all of his rejections of the independent claims. Such Official Notice is improper and clearly not in accordance with MPEP 2144.03A&B; *"It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. Zurko,* 258 F.3d at 1385, 59 USPQ2d at 1697 {emphasis added}. See, e.g., the discussion of Claim 40 (Par. 86 of the Office Action) in Item (iii) below for but one example of how such Official Notice is improperly used as a principal basis of rejection in the Office Action.

Also, as previously noted, Official Notice comprises the basis for rejection of every independent claim in the application. It stretches credibility beyond all bounds to say that none of these uses comprises a "principal" basis for rejection as proscribed by MPEP 2144.03A&B.

Furthermore, the Examiner's repeated citation of Official Notice throughout the Action for the proposition that "DRAM and its advantages are well known and expected in the art" (see, e.g., Par. 42, regarding Claim 1) comprises an improper use of Official Notice pursuant to MPEP 2144.03 A-C. Applicant's invention of, e.g., Claim 1 utilizes a specific optimized architecture including an embedded DRAM processor that interfaces directly to DRAM. See also, e.g., Claim 28, which is directed specifically at an embedded DRAM processor that is moving entire rows of the DRAM array to/from a register file in parallel.

The Examiner's use of Official Notice in this instance is akin to asserting that a hypothetical claimed monoplane (single wing aircraft) is obvious over (i) bi-plane prior art, combined with (ii) Official Notice that "use of a wing" is well known. Clearly, the invention of the monoplane required additional inventive novelty and inventive step over the bi-plane prior art. The entire architecture of the claimed monoplane (e.g., wings, fuselage, landing gear, etc.) is adapted specifically for a craft with a **single** set of wings. Hence, the Official Notice of "a wing" is improperly used as the primary basis of the rejection, being "boot-strapped" to the bi-plane art to ostensibly teach or suggest something which it clearly does not (i.e., an aircraft with a single set of wings capable of flying).

In the present context, the Examiner's Official Notice that "DRAM and its advantages are well known and expected in the art" is being boot-strapped onto Inagami (US 4,881,168), which teaches nothing of DRAM, to ostensibly form Applicant's claimed invention, thereby improperly using such Official Notice as the primary basis for rejection. Stated differently, without this Official Notice, the Examiner's obviousness arguments fall apart, since Inagami does not teach anything to do with DRAM.

**Per MPEP 2144.03C, Applicant hereby requests that the Examiner provide explicit references that teach an embedded DRAM processor with the functionality of the claimed inventions, since the Examiner has failed to do so to this point.**

(iii) **Improper Standards Applied in Use of "Official Notice"** – Yet in addition to the foregoing, Applicant submits that the Examiner has utilized an improper standard in all instances of his Official Notice; i.e., the "facts" that the Examiner cites as being well known are clearly related to the state of the art and subject to argument. MPEP 2144.03A states:

> *"It would **not** be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must **always** be supported by citation to some reference work recognized as standard in the pertinent art. In re Ahlert, 424 F.2d at 1091, 165 USPQ at 420-21. See also In re Grose, 592 F.2d 1161, 1167-68, 201 USPQ 57, 63 (CCPA 1979) ... In re Eynde, 480 F.2d 1364, 1370, 178 USPQ 470, 474 (CCPA 1973) ("[W]e reject the notion that judicial or administrative notice may be taken of the state of the art. The facts constituting the **state of the art** are*

*normally subject to the possibility of rational disagreement among reasonable men and are **not** amenable to the taking of such notice.")."* {Emphasis added}

A most illuminating example on this point is the Examiner application of Official Notice to those of Applicant's claims discussing generally data movement operations that interfaces directly to DRAM, (e.g., performing data move operations on the cache-DRAM type register file prior to switching the cache-DRAM type register file into an architectural register set). In this specific context, it is clearly improper to use Official Notice to support a blanket rejection of "register-register move operations are well known...."; see e.g., Par. 86 of the Office Action relating to Claim 40. Applicant agrees that data move operations generically are well known, but not in the context of Applicant's invention of Claim 40; i.e., an embedded DRAM processor that interfaces directly to DRAM. Per MPEP 2144.03C, **Applicant hereby requests that the Examiner provide explicit references that teach such functionality in the context of an embedded DRAM processor, since the Examiner has failed to do so to this point.**

Based on items (i)-(iii) above, Applicant submits that the Examiner has improperly utilized all instances of Official Notice in rejecting, *inter alia*, Claims 1, 13, 16, 23, 28, 40, 43, 45, 46, 48 and 49 (as well as their dependent Claims), and that all such rejections predicated on "Official Notice" (whether explicit or implicit) must be withdrawn.

2) Characterization and Use of the Prior Art

The Examiner is respectfully reminded that proper patent examinations and proper rejections must rely on the written record of the prior art, not subjective opinion or determination.

When prior art is used, the prior art must be properly characterized and taken in proper context, and only combined when there is a proper reason or motivation to combine (see MPEP 2143). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Prior art that teaches away from the invention under Examination cannot be relied upon merely because it happens to contain a stray word relative to an element of the claimed invention.

3) Distinctions Over the Prior Art

(i) Per Par. 41 of the Office Action, Claims 1, 6-10,12-15 and 46-48 were rejected under Section 103(a) over Inagami (US 4,881,168), and Wright (US 5,587,961), as well as "Official Notice".

**Claims 1, 13, 46 and 48**- By this paper, Applicant has amended independent Claims 1, 46 and 48 to include limitations relating to precharging functionality of the claimed processors. See, *inter alia*, Applicant's specification at page 26, line 24 to page 27, line 6 for support.

Claim 1 describes a system that enables precharging. The row register address register of the claimed invention is wholly different from the vector address register 60 of Inagami because the row register address register of the present invention can be used (for example, as an operand in DRAM row-based applications) in precharge-row and deactivate-row instructions. For example, one possible use of this functionality (although by no means an exclusive or only use) is to speculatively precharge a row before it is actually used. The row can be speculatively precharged in advance of one or more load/store operations. Subsequently, a long string or a shorter burst of load store operations can be performed without the need to keep recharging the row. This improves the effective bandwidth of the DRAM. After the program no longer needs to access the row, the deactive instruction can be given and another row can be precharged. When multiple banks of DRAM are available, the data assembly unit can precharge different rows in different banks of DRAM. **Neither Inagami, nor any of the other cited art) teach or suggest such pre-charging functionality in any way.**

The SDRAM commands in Wright are hardware layer memory commands sent directly to the DRAM device, and hence Wright does not teach or suggest the use of the use of a row address register nor a precharge command nor a deactivate command as taught by Applicant.

Applicable portions of the foregoing distinctions are relevant to Claim 46 as well.

Claim 48 has been amended herein to include limitations relating to the recited loading of selected columns of rows pointed to by the recited row address registers into designated sets of said data registers being performed in response to an instruction issued **after** the precharging. Inagami '168 in no way teaches or suggests load/store operations that are in response to an instruction issued after precharge.

In fact, under the Examiner's assertions of "Official Notice" relating to DRAM, the load/store instruction itself would comprise the "precharge" instruction, and hence Inagami combined with the Examiner's Official Notice clearly *teaches away* from Claim 48 as amended herein.

**Claim 13**- By this paper, Applicant has amended independent Claim 13 to include limitations relating a command to precharge that is executed to precharge a precharged row prior to the recited command to load so that at the time the command to load is issued, the command to load can execute without the need to wait for the designated row to precharge. See again, *inter alia*, Applicant's specification at page 26, line 24 to page 27, line 6, for support for these limitations. **None of the cited art, including Inagami and Wright, teach or suggest such functionality in conjunction with the other limitations of Claim 13.**

Accordingly, Applicant submits that Claims 1, 13, 46, and 48, and all claims that depend directly or indirectly therefrom, are novel and non-obvious over the cited art, and in condition for allowance.

(ii) Per Par. 55 of the Office Action, Claims 2-5, 11 and 16-27 were rejected under Section 103(a) over Inagami (US 4,881,168), in view of Parady (US 5,933,627), as well as "Official Notice".

**Claim 16** - By this paper, independent Claim 16 has been amended to include limitations relating to a set of functional units that perform logical operations on data accessed from a set of architectural registers, wherein registers placed into the active state appear as architectural registers to a set of functional units, and registers in the inactive state the registers are not accessible by the functional units. Paraday in no way teaches or suggests executing a command on the inactive registers to load the inactive register set while the functional units are busy accessing the active register set as the architectural registers; see element (ii) of Claim 16.

**Claim 23** – Subject to amendments made herein, Applicant traverses the Examiner's Section 103 rejection of Claim 23 in that, *inter alia*, there is no teaching or suggestion in Inagami, Paraday (or for that matter Wright) or any combination thereof (including the Examiner's traversed "Official Notice" citation), to provide a processor architecture that includes

(i) a row address register that points to DRAM rows, (ii) commands to manipulate the DRAM row address pointer, and (iii) a load command to write an entire DRAM row into a register file. Applicant requests that the Examiner provide citations for such teachings; i.e., showing writing an entire DRAM row.

Accordingly, Applicant submits that Claims 16 and 23, and all claims that may depend therefrom, define patentable subject matter and are in condition for allowance.

(iii) Per Par. 73 of the Office Action, Claims 28-45 and 49 were rejected under Section 103(a) over Inagami (US 4,881,168), in view of Parady (US 5,933,627) and Bissett (US 5,896,523), as well as "Official Notice".

**Claim 28, 45 and 49** – Claim 28 as presented herein recites "a command to unidirectionally transfer data between a row of said DRAM array and a selected inactive data register file". No teaching or suggestion of this functionality is present in Inagami '168. Inagami utilizes a vector address register and obtain four words at a time from main memory. The concept of moving data between a load store unit and an inactive register file (for example, while a different thread is active), is completely absent from Inagami.

Furthermore, there is no suggestion or motivation to combine Paraday with Inagami because the vector processor of Inagami in no way needs to perform such operations involving use of an inactive register file (such as, e.g., relating to the aforementioned thread switching). The Examiner is directed the Applicant's disclosure at page 24, line 6, to page 26 line 4; see especially page 24, lines 18 to 29.

Paraday (US 5,933,627) teaches to use the active/inactive registers so that different threads can switch so the register state need not be saved. The Paraday reference simply does not teach using registers for the purpose of the invention of Claim 28, i.e., to transfer data to/from one register set to load/unload, while a set of functional units utilize the other register set. There would be absolutely no motivation to combine Paraday's register files, which are designed for fast thread switching, to arrive at the applicants invention of an embedded-DRAM processor that allows (e.g., single thread) movement of data into and out of a DRAM efficiently to keep the functional units of a processor substantially utilized.

Applicant further notes that Inagami uses "parallel-by-element processing"; an individual vector instruction will specify processing for all of the operational pipelines, or will specify all the processing for many cycles of operational processing, or will specify both load store operations and operational processing. The use of parallel-by-element processing in Inagami clearly teaches away from Applicants invention of Claim 28 as presented herein. "*If the proposed modification or combination of the prior art would change the **principle of operation** of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious.*" MPEP 2143.01 {emphasis added}

Applicant yet further notes that in the invention of Claim 28, the data movement unit is able to move data between the DRAM array and the inactive register file while a different register set is utilized as the active register set that appears as architectural registers to a corresponding set of functional units. In contrast, Paraday teaches multiple register sets that are either active or inactive, thereby further teaching away from Applicant's invention of Claim 28.

Similar arguments apply to independent Claims 45 and 49.

Accordingly, Applicant submits that Claims 28, 45 and 49, and all claims that may depend therefrom, define patentable subject matter and are in condition for allowance.

*New Claims*

By this paper, Applicant adds new Claim 50. Applicant submits that Claim 50 is fully supported by the specification and drawings as filed, and comprises patentable subject matter.

*Other Remarks*

Applicant hereby specifically reserves all rights of appeal, as well as the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention and responding to the aforementioned Action, and not for purposes of overcoming art or for patentability. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such claim cancellations or additions.

Furthermore, any remarks made with respect to a particular claim or claims shall be limited to only such claim or claims.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: 5/9/05

By: _____

Robert F. Gazdzinski
Registration No. 39,990
11440 West Bernardo Court, Suite 375
San Diego, CA 92127
Telephone No.: (858) 675-1670
Facsimile No.: (858) 675-1674